RollNo.

ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

CONTROLLER OF EXAMINATIONS ★ ADDITIONAL ★ AU CHENNAI 600 025

B.E. /B.Tech / B. Arch (Full Time) - END SEMESTER EXAMINATIONS, May 2024

Name of the Branch: Electronics and Communication Engineering
Semester: VI
Subjectcode&SubjectTitle: EC5015- Data Converters
(Regulation2019)

Time:3hrs Max.Marks: 100

CO1	To design MOS circuits applied for various data conversion stages namely, sample and hold, comparators, switched capacitor amplifiers
CO2	To, study the various CMOS design considerations of ADC architectures used in practice• including SAR, Pipeline, Flash ADCs
CO3	To study the general design principles design sigma delta converters•

BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	In Fig.1 briefly explain how the ratio Ts/Tp should be chosen and whether this is an issue in the context of ADCs or in the context of DACs or both.	2	1	L2
2	A full scale sinusoidal input is sampled and quantized using a 10 bit ADC and two sets of data are collected. The FFT plots of these two data sets are shown in Fig.2a and Fig.2b. What could be the reason for the two plots to appear different.	2	1	L4
3	For a typical T/H circuit shown in Fig.,3a the output waveforms are observed as shown in Fig3b. Explain why there is a difference between the ideal and actual waveforms at the output of the T/H circuit.	2	1	L2
4	Determine the expression for SNR due to jitter for an input $x(t) = A\cos(2\pi ft)$ and a sampling clock jitter variance given by $(\sigma_t)^2$.	2	1	L1
5	Explain what is kick back effect in comparators.	2	1	L1
6	Briefly explain any one circuit scheme which will help reduce the offset voltage of a comparator.	2	1	L1
7	"In a Sigma Delta A/D converter, if the Over Sampling Ratio (OSR) is increased, the order of the aniti alias filter prior to ADC also must be increased to obtain the same performance as before". State with justification if this statement is true or false.	2	3	L2
8	For the circuit in 4a along with the waveforms in Fig.4b, determine the relation between $V_{out}[n]$ and $V_{in}[n]$.	2	3	L4
9	Briefly compare the speed of operation of SAR ADC and a pipeline ADC	2	2	L4
10	Explain under what conditions glitch error can be made zero in binary coded current steering DACs.	2	2	L1

PART- B(5x 13=65Marks)
(Restrict to a maximum of 2 subdivisions)

Q.No	Questions	Marks	CO	BL
11 (a) (i)	The quantization error plot of an ADC for a ramp input is of the form shown in shown in Fig. 5. Determine the average power in this waveform over one period.	(4+9)	1	L5
11 (a)(ii)	Consider the current mirror circuit shown in Fig.6 which is modeled to show the mismatches in the transistors. For the process, assume that A_{Vt} = 5mV-um and $A_{\Delta\beta/\beta}$ = 1%um. Assume for this current mirror, W1 = W2 = 500um and L1=L2=50um. Determine the standard deviation $\sigma_{\Delta I/I}$ of the fraction deviation of the current.			

	OR			
11(b)	The ideal transfer characteristic of a DAC are shown in Fig.7. Sketch and show how this figure would get modefied in the presence of (i) gain only and (ii) offset errors only. Define the terms, missing codes, DNL and INL in the context of an ADC. Explain why spectral leakage occurs while taking the FFT of ADC output samples.	**((3+2+ 2+2+2 +2)**	1	L5
12 (a)	Consider the equivalent circuit for the T/H shown in Fig. 8a and the step input waveform shown in Fig 8b. Determine the number of time constants N one has to wait such that the tracking error is less than ½ LSB in a 10 bit quantizer. Assume $N\tau = fs/2$ where fs is the frequency of the clock signal Φ. Next consider the same T/H circuit is fed with an input $Vin = A\cos(\omega t+\Phi)$ as shown in Fig.8c. The corresponding output obtained is given by the expression $V_{out}(t) = -\frac{A\cos(\phi-\theta)}{\sqrt{1+\omega^2\tau^2}}e^{-\frac{t}{\tau}} + \frac{A\cos(\omega t+\phi-\theta)}{\sqrt{1+\omega^2\tau^2}}$ where $\vartheta = \tan^{-1}(\omega\tau)$. Assume $\omega = 2\pi/(N\tau/2)$. If the output for this case is sampled after N time constants where N is the value that you have determined for the step input in this question, what is th percentage error in the output amplitude. How many bits of precision could this correspond to.	**(5+4+ 4)**	1	L4
	OR			
12 (b) (i)	The circuit in Fig.9 shows depicts the equivalent circuit for a T/H circuit. Write down the expression for the value of the clock waveform Φ at which the MOSFET turns OFF. Assuming slow gating and ignoring charge injection, express the Vout as $Vout = Vin(1+\varepsilon) + Voff$ and determine the expressions for ε and Voff. Further, assuming C=1pf, Mosfet parameters as Vth = 0.45V, W =20um, $C_{OL} = C =$ 2fF, determine the values of ε and Voff. Assume that the clock low voltage $\Phi_L = 0V$.	**3+2+2 +2**	1	L4
12(b) (ii)	Distinguish between fast gating and slow gating in the context charge injection error and give the expression for charge injection output error voltage for the fast gating case.	**4**		
13 (a) (i)	Explain the operation of the circuit shown in Fig.10 under clk = 0 and clk =Vdd conditions. Mark suitable the input terminals Vinp ad Vinn and Vop and Von. Why are there so many capacitors shown on the left and right	**5+2**	1	L3
13(a) (ii)	Explain the operation of the circuit in Fig.11. Mark the output terminals $Vout^+$ and $Vout^-$ appropriately.	**4+2**		
	OR			
13 (b) (i)	Write down the possible first order differential equations for the comparator circuit shown in Fig.12. Assume Vs1 and Vs2 as the logic threshold voltages for the two inverters.	**6**	1	L3
13(b) (ii)	In part 13b(i) above, assume that C1 = C2, Gm1=Gm2, Cc = 0 and solve the differential equation and show that the output will grow exponentially with time.	**7**		
14 (a) (i)	For a Noise Transfer Function of the type $H_E(z) = (1-z^{-1})^L$, show that doubling of the Oversampling Ratio M increases the SQNR by a factor 6L+3dB.	**8**	3	L3
14 (a) (ii)	For the block diagram shown in Fig.13, obtain transfer function between $Y(z)/\varepsilon_{DAC}(z)$. Based on this, comment on the bit precision of the DAC in comparison to the bit precision of the quantizer in the loop as well as the overall bit precision of the ADC.	**3+2**		
14 (b) (i)	Show that the SQNR for the ciruit shown in Fig.14 is given by SQNR = -3.4+30log(M) dB where M is the oversampling ratio.	**7**	3	L3
14(b) (ii)	For the circuit in Fig.15 assume M=128 and the input signal frequency is 20kHz. At the output of the digital filter, what is the possible value of B and what could be the minimum possible rate at which this data can come out of the digital filter.	**4+2**		
15 (a)	Draw the complete circuit diagram of a two bit pipeline ADC. Explain the full circuit operation and discuss the function and operation of the multiplying	**5+4+4**	2	L3

	DAC in this case.			
	OR			
15 (b) (i)	Draw the complete circuit diagram of 3 bit SAR ADC With the help of an equivalent circuit and appropriate charge conservation equations, explain the circuit operations during the input sampling phase and any one reference comparison phase. What are the possible sources of error in SAR ADC.	**6+7**	2	L3

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No	Questions	Marks	CO	BL
16. (i)	Consider the AD converter model and FFT setup shown in Fig.16. Assume Vin = $A*\sin(2\pi f_{in}t)$, A= 0.7V, f_{in} = 577MHz, fs =1024MHz, The quantizer is ideal and has a full scale range of 2V (+/- 1.0Volts). Assume initially N(k) = 0 for all k. Calculate the SNR in dB that will measured for this case. Assuming the FFT plot is given from 0 to fs/2, what will be frequency of the sine wave indicated by the FFT plot. Assume next that the N(k) represent Gaussian white noise samples of zero mean and standard deviation 2mV. What will be the SNR measured at the out for this nonzero N(k) case.	**7+8**	1+3	L5+L6
16 (ii)	The model of a Sigma Delta converter is shown in Fig 17 in which the analog input of the single quantizer (A) is fed as input to the N bit quantizer (B). The quantized signals are then filtered and combined to produce the output. Assume that the loop filter is an ideal integrator Ha(z) = 1/(z-1). Determine an expression for the output Y(z) in terms of X(z), E1(z), E2(Z), Ha(z), H1(z) and H2(z). Determine H1(z) and H2(z) such that E1(z) no longer appears at the output and only E2 is first order noise shaped.			

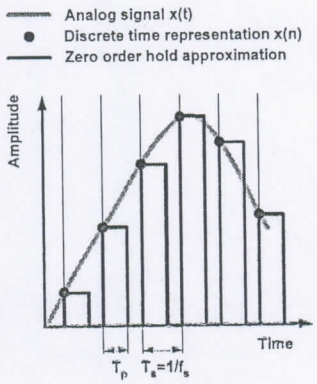

Fig.1

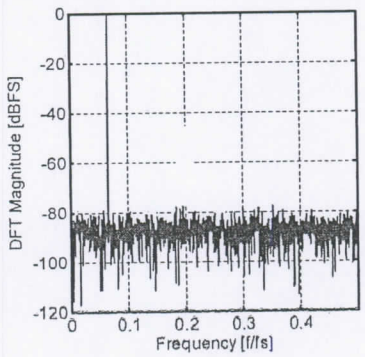

Fig.2a

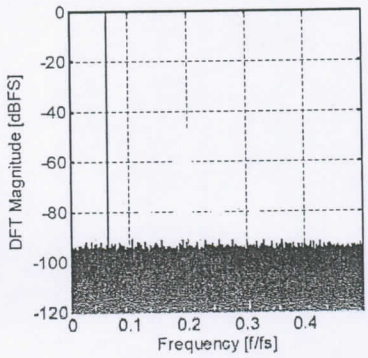

Fig.2b

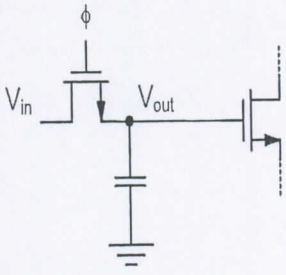

Fig.3a

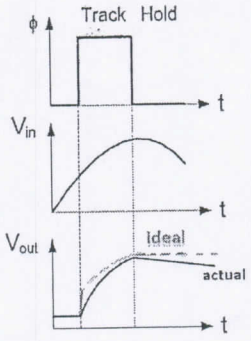

Fig.3b

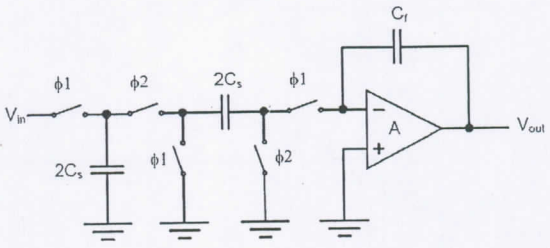

Fig.4a

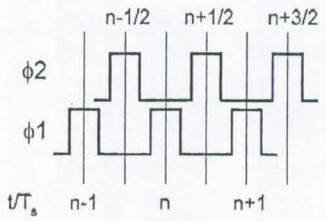

Fig.4b

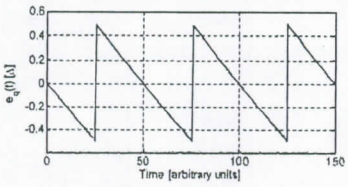

Fig.5

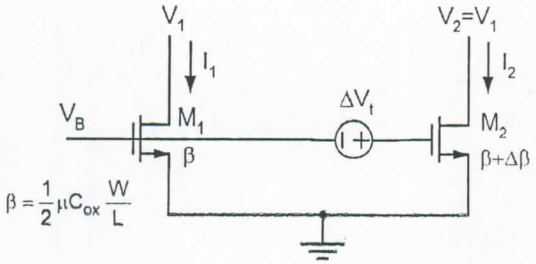

Fig.6

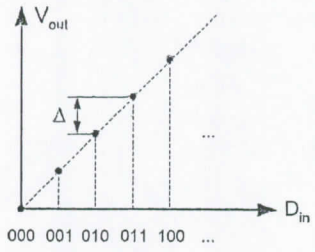

Fig.7

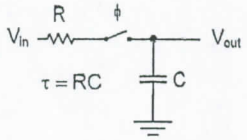

Fig.8a

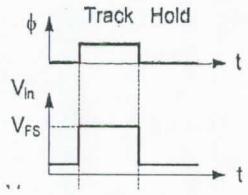

Fig.8b

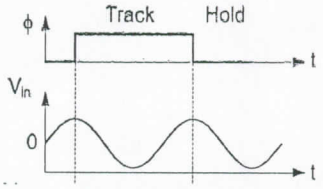

Fig.8c

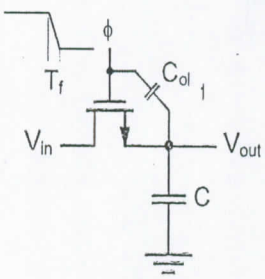

Fig.9

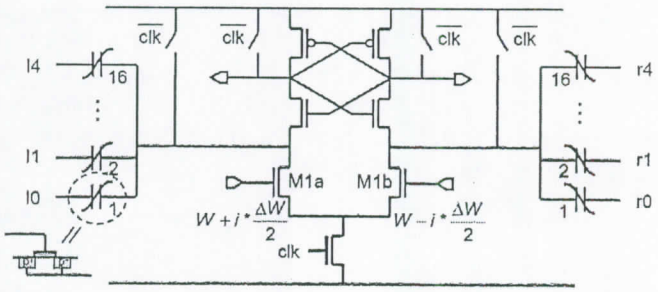

Fig.10

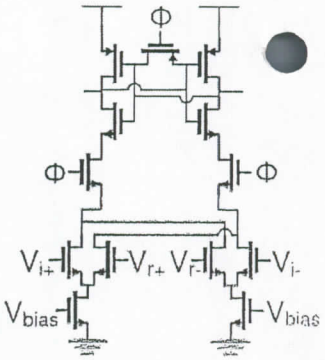

Fig.11

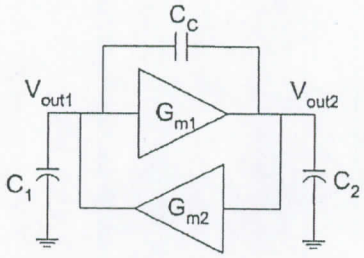

Fig.12

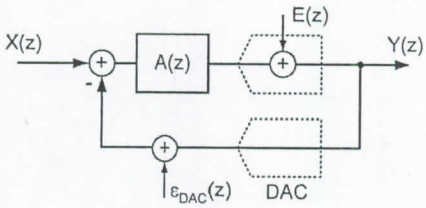

Fig.13

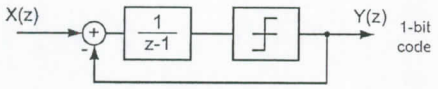

Fig.14

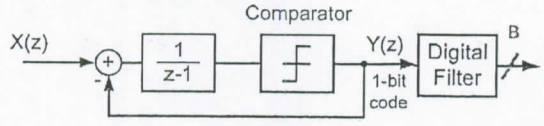

Fig.15

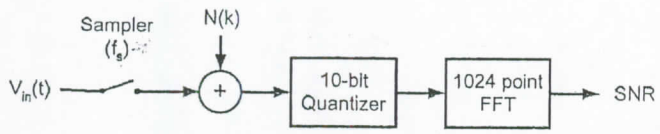

Fig.16

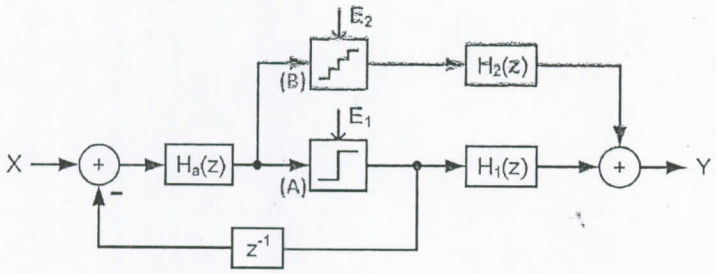

Fig.17